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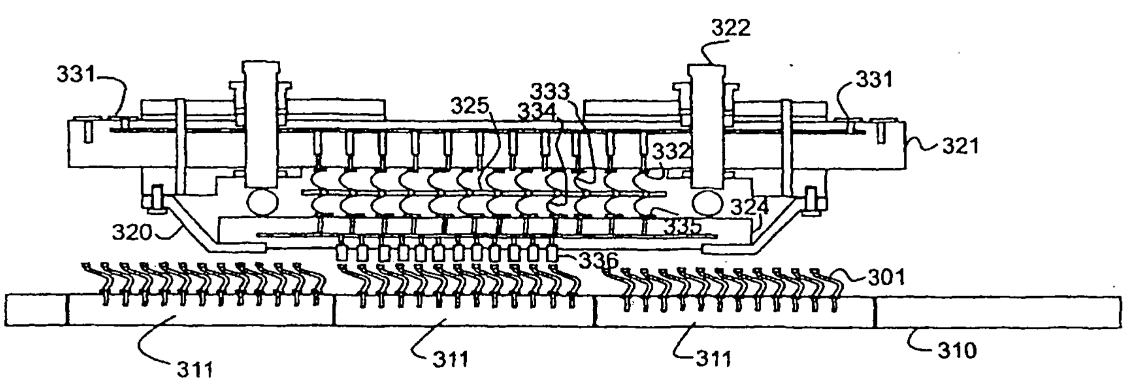

(57) Abstract

A probe card is provided for contacting an electronic component with raised contact elements. In particular, the present invention is useful for contacting a semiconductor wafer with resilient contact elements, such as springs. A probe card is designed to have terminals to mate with the contact elements on the wafer. In a preferred embodiment, the terminals are posts. In a preferred embodiment the terminals include a contact material suitable for repeated contacts. In one particularly preferred embodiment, a space transformer is prepared with contact posts on one side and terminals on the opposing side. An interposer with spring contacts connects a contact on the opposing side of the space transformer to a corresponding terminal on a probe card, which terminal is in turn connected to a terminal which is connectable to a test device such as a conventional tester.

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PROBE CARD FOR PROBING WAFERS WITH RAISED CONTACT ELEMENTS

Field of the Invention

This invention is directed to an apparatus for contacting an electronic component with raised contact structures. This invention is particularly well suited for probing wafers with resilient contact structures.

Background of the Invention

It is well understood in the art of manufacturing semiconductor devices to test devices while still unsingulated from the wafer for some level of functionality. Conventionally this is done using a probe card and a prober. A representative probe card is illustrated in Figure 1. The probe card is mounted in a prober, which in turn detects with high precision the position and orientation of the probe card, and the position and orientation of a wafer to be tested, then brings the two into precise alignment. The probe card is connected in turn to a tester, providing a connection between the tester and one or more devices on the wafer. The tester can energize the device under test (DUT) and evaluate the performance of the device. This process is repeated as needed to test substantially each device on the wafer. Devices which pass the test criteria are processed further.

One particularly useful probe card makes use of resilient spring elements for contacting the wafer. Such a probe card is illustrated in Figure 1. This probe card is described in detail in commonly assigned United States Patent No. 5,974,662, entitled "Method of Planarizing Tips of Probe Elements of a Probe Card Assembly," and the corresponding PCT Application published May 23, 1996 as WO 96/15458.

Semiconductor devices are manufactured on a semiconductor wafer but must be singulated and connected to external devices in order to function. For many years, the standard method of connecting a semiconductor has involved fabricating a semiconductor device with pads, typically of aluminum. These pads are connected to larger structures, typically a lead frame, typically using wirebonding. The lead frame can be mounted in a suitable package, typically of ceramic or plastic. The spacing of connections on the package is designed to mate with a circuit board or other mating device such as a socket. Various innovations in packaging over the years allow for relatively close spacing and ever-higher pin counts in packaging.

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A significant change from this packaging paradigm is seen in BGA packaging. Here, the contact points are globules of a reflowable material. A solder material is commonly used, so that a package can be positioned at a contact area then heated to reflow the solder, providing a secure electrical connection. This same general strategy is used at the chip level, forming small bumps over contact areas. A commonly used process makes C4 balls (controlled collapse chip connection).

Conventional probe cards are designed to contact traditional bond pads, typically aluminum. The novel probe card of Figure 1 is useful for this purpose. Probing C4 balls is more complex for a variety of reasons, but the probe card of Figure 1 is particularly well suited for this purpose as well.

A new form of packaging has become available which allows formation of small resilient contact structures directly on a semiconductor wafer. This is the subject of several patents, including United States Patent 5,829,128, issued November 3, 1998. An illustrative embodiment is shown here in Figure 2 as wafer 208 with springs 224 connected to terminals 226.

A large scale contactor has been disclosed for contactor some or all of a semiconductor wafer which is built with resilient contact elements. Fixturing and burn-in processes are described in copending, commonly assigned United States patent application Serial No. 08/784,862, filed January 15, 1997, which is incorporated herein in full by reference. The corresponding PCT application was published as WO 97/43656 on November 20, 1997.

Summary of the Invention

The present invention provides a probe card useful for probing a semiconductor wafer with raised contact elements. In particular, the present invention is useful for contacting resilient contact elements, such as springs.

A probe card is designed to have terminals to mate with the contact elements on the wafer. In a preferred embodiment, the terminals are posts. In a preferred embodiment the terminals include a contact material suitable for repeated contacts.

In one particularly preferred embodiment, a space transformer is prepared with contact posts on one side and terminals on the opposing side. An interposer with spring contacts connects a contact on the opposing side of the space transformer to a corresponding terminal on a probe card, which terminal is in turn connected to a terminal which is connectable to a test device such as a conventional tester.

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It is an object of this invention to provide a probe card for probing a semiconductor device with raised contact elements.

It is another object of this invention to probe card an electronic component with raised contact elements. Such an electronic component can include a packaged semiconductor such as a BGA package.

This and other objects and advantages of the invention, as well as the details of an illustrative embodiment, will be more fully understood from the following specification and drawings.

Brief Description of the Drawings

Figure 1 illustrates a probe card for probing conventional semiconductor devices.

Figure 2 illustrates a probe card for probing semiconductor devices with raised contact elements.

Figure 3 illustrates a second embodiment of a probe card for probing semiconductor devices with raised contact elements.

Figures 4 through 9 illustrate steps in the process of forming a post suitable for use in the probe card of this invention.

Figures 10 and 11 illustrate the apparatus of the invention used with a wafer including travel stop protectors.

Description of the Preferred Embodiments

The probe card assembly of Figure 1 has been described in detail in commonly assigned United States Patent No. 5,974,662, cited above. This figure is Figure 5 in the 5,974,662 patent, using reference numbers in the 500 series, renumbered here in the 100 series.

Referring to Figure 2, the probe card assembly of Figure 1 has been modified slightly for the new purpose. Common elements include supporting probe card 102 which is mounted into a prober (not shown). Interposer 112 includes springs 114 and corresponding springs 116 which connect through the interposer so that corresponding terminals 110 and 120 are electrically connected. In space transformer 106, corresponding terminals 120 and 222 (122 in Figure 1) are connected. Probe card 102 supports connecting circuitry so a tester lead can be connected to a corresponding terminal 110, and then through 114, 116, 120 and 222 (or 122) to receive a connection

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from a semiconductor device. In Figure 1, resilient contact element 124 is connected to terminal 122, and is brought into contact with terminal 126 on semiconductor wafer 108. In Figure 2, semiconductor wafer 208 has terminals 226 which in turn have raised contact elements, here resilient contact elements 224, which can be brought into contact with corresponding contact regions of corresponding terminals 222 to complete a circuit to the tester. The tester can energize a connected semiconductor device and evaluate the functionality of the device.

Interposer 112 with springs 114 and 116 pushes against terminals 110 and 120. By compressing the space transformer 106 towards the probe card 102 against the spring forces of interposer 112, the interposer will maintain contact with each corresponding terminal 110 and 120 even if the planarity of the tips of springs 114, of springs 116, of terminals 110 and of terminals 120 are imperfect. Moreover, within the limits of resiliency of the various components, the space transformer can be angled relative to the probe card to allow for alignment in certain dimensions. Differential screws 138 and 136 can be adjusted very precisely to reorient the surface of space transformer 118 relative to probe card 102. Consequently, anything connected to the space transformer correspondingly will be oriented. Thus the tips of springs 124 in Figure 1 and the terminals 222 in Figure 2 can be positioned with high accuracy relative to a semiconductor wafer.

Referring to Figure 3, the components of Figure 2 can be seen in an alternative embodiment. The primary elements function as described in relation to Figure 2. Space transformer 324 supports terminals 336 and 335, which are connected appropriately. Interposer 325 supports resilient contact elements 334 and 333. Probe card 321 supports terminals 332 and 331, which are connected appropriately. In general, a lead from a tester will connect to a terminal 331, which is connected in turn to a terminal 332, then through resilient contact elements 333 and 334 to a terminal 335 and finally to a corresponding terminal 336. Support spring 320 holds the space transformer 324 against interposer 325 and probe card 321. Orienting device 322 functions as described above to refine the orientation of the space transformer relative to the prove card 321.

Figure 3 shows a broader view of semiconductor wafer 310, here with several distinct semiconductor devices 311. Here a single semiconductor device is shown almost connected with corresponding terminals 336. By moving semiconductor wafer 310 towards probe card 321, a microspring contact 301 is brought into direct and intimate contact with a contact region of a corresponding terminal 336, and connected therefore to a corresponding tester lead. After testing, the semiconductor wafer can be repositioned to

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bring another semiconductor device into contact with the corresponding terminals on the probe card assembly.

Figure 4 illustrates a particularly preferred method of fabricating a post structure. Details of fabricating the interposer, space transformer, and probe card are detailed in commonly assigned United States Patent No. 5,974,662, and earlier applications cited there.

Referring to Figure 4, in structure 400 a support substrate 405 includes terminal 410, interconnection 420, and terminal 415. Suitable materials and alternative compositions are detailed in the referenced applications. For a preferred embodiment, the support substrate is a multilayer ceramic substrate. A conductive layer 417 connects a plurality of terminals 415 (other terminals not shown). A more detailed description of the following steps can be found in copending, commonly assigned application entitled "Lithographic Contact Elements", United States Patent Application Serial No. 09/205,423, and corresponding PCT Application filed November 23, 1999, Serial No. <not yet known>. Figures 4 through 7 are adapted from Figures 1 through 4 of that corresponding application.

In the process of electroplating, it is advantageous to provide a common connection between elements to be plated in order to provide a suitable circuit for plating. Other methods of deposition may be used to form structures similar to the one described here. Such methods are described or references in USPN 5,974,662 and supporting applications. One alternative to a shorting layer such as 417 is to provide a shorting layer 407 directly connecting a plurality of terminals 410 (only one shown here). Both are shown here but in practice generally only one or the other would be used. Use of a "top" layer such as 407 is particularly advantageous when there is no convenient way to connect through the substrate. Such might be the case when using silicon as a substrate, or certain configurations of ceramic, polyimide, or other materials.

Shorting layer 407 is applied by sputtering. Details of materials, thicknesses, processing variations and the like can be found in corresponding, commonly assigned United States Patent Application 09/032,473, filed February 26, 1998, entitled "Lithographically Defined Microelectronic Contact Structures," and corresponding PCT application, published as WO 98/52224 on November 19, 1999, both of which are incorporated herein in full by reference. One particularly preferred material is an alloy of tungsten and titanium. This can be applied by sputtering. A useful depth is on the order of 3,000 to 6,000 Angstroms, such as about 4,500 Angstroms. Various alloys of titanium or of tungsten also are useful.

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A layer of resist such as a negative photoresist 425 is applied to the surface of the substrate (on top of any other applied layers, of course). This is patterned to leave an opening over terminal 410.

A suitable structural material 430 is deposited in the opening in the photoresist, more than filling the opening. In a preferred embodiment, a material such as an alloy of nickel and cobalt is deposited by electroplating. Other useful materials include copper, palladium, palladium cobalt, and alloys including these materials. Other deposition methods such as sputtering may be suitable.

A lapping or grinding process such as chemical-mechanical polishing is used to remove excess structural material to leave a highly planar structure. Moreover, other structures on the substrate are planarized. It is desirable to have minimal height deviation both in the region of a single post as well as over a series of posts. Flatness on the order of one in 1,000 (height above surface measured at relatively distant corresponding feature) is desirable although the specific constraints of a given design may well allow for 2 to 5 to 10 in 1,000 or even more. This corresponds to a height consistency of about 100 microinchs per linear inch or about 1 micron per centimeter.

In one preferred embodiment an additional contact layer is applied. Referring to Figure 8, a contact layer 431 is deposited onto structural material 430. In one preferred embodiment, this is deposited by electroplating. A preferred material is an alloy of palladium and cobalt. Other useful materials include palladium, hard gold, soft gold and rhodium. The thickness can be chosen by design criteria understood by those skilled in the art of making contact components. In one preferred embodiment the thickness is from about 0 to about 200 microinches (about 0 to about 5 microns).

The structure is finished by stripping the masking layer of photoresist, and removing the conductive layer 407 or 417. Useful techniques include ashing, wet etch and laser ablation. Details of time, materials and conditions are extremely well known in the art. Referring to Figure 9, the finished structure 400 then can be incorporated in a probe card assembly as shown in Figure 2 or 3.

The geometries of the terminals are quite flexible using this method and the designer has a great degree of flexibility. It is quite simple to form posts which are approximately square in cross section (in the XY plane substantially parallel to the substrate surface). This can be on the order of about 1 to 10 mils in each of the X and Y dimensions. Obviously almost any size and shape can be designed here. It is convenient to make the height of the structure on the order of 0 to 60 mils (0 to 1.5 millimeters) away from the substrate surface. Of course the terminal can actually be recessed below

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the surface of the substrate so long as the terminals collectively are highly planar. A useful height is on the order of about 5 to about 10 mils (125 to 250 microns). Another preferred embodiment includes structures which have a height on the order of about 40 to 60 mils (about 1 to 1.5 millimeters).

Orienting the probe structure so it is aligned as well as possible with the plane of the wafer to be tested is very beneficial. Having the surface of the space transformer reasonably flat is very helpful as well. Assuming that the contact ends of the resilient contact structures on the wafer ("tips" in one perspective) are generally co-planar, bringing coplanar tips into contact with coplanar terminals across aligned planes means that the tips can be depressed a minimal amount in order to guarantee contact of all tips with all terminals. Whatever amount of non-coplanarity exists in the tips, in the terminals, or in mis-alignment of the planes for contact gives the result that some portion of the tips will have to travel further in order to guarantee that all tips are in satisfactory contact. The structure described here can readily be made relatively flat and oriented successfully to allow minimal drive on the wafer. In a preferred design, an over travel on the order of 3 mils (75 microns) is one useful design point. That is, from the point where the first tip touches a corresponding terminal, the base corresponding to that tip is driven the over travel distance closer to the terminal. This compresses the tip against the terminal and, in many designs, causes the tip to slide across the terminal, thus digging into and through any contaminants that may be present on either the tip or the terminal. This also drives other tips into contact with and along corresponding terminals. If components are properly designed and aligned, the selected degree of overtravel will cause the tip which is last to contact a corresponding terminal still to be able to establish a suitable contact.

Some instances of wafers with springs include an overtravel stop protector. Such overtravel stop protectors are described in detail in copending, commonly assigned United States Patent Application Serial Number 09/114,586, filed July 13, 1998, entitled "Interconnect Assemblies and Method", naming as a sole inventor Benjamin Eldridge and corresponding PCT Application Serial No. US 99/00322, filed January 4, 1999. Referring to Figure 10, one example of such an overtravel stop protector can be seen. Semiconductor wafer 1008 is fabricated to include terminals 1026, with resilient contact elements 1024. Compare 208, 226 and 224 in Figure 2. In addition, an overtravel stop protector 1025 is included. In one preferred embodiment this takes the form of a cured epoxy. The protector can take many forms. As illustrated, the protector is more or less a field of epoxy, generally planar, with openings only for the resilient contact elements 1024. The height of the stop protector is selected so each resilient contact element can deform the desired amount but then will pass "below" the level of the protector,

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effectively limiting overtravel. A wafer with such stop protectors can be tested using the same apparatus described above in Figures 2 and 3.

Referring to Figures 10 and 11, as the resilient contact elements 1024 first contact corresponding terminals 222, the resilient contact elements first touch the corresponding terminals then begin to wipe across the surface. In Figure 11 the resilient contact elements 1024A are in contact and have been compressed to some degree. In Figure 11, each terminal 222 has come into contact with a corresponding overtravel stop protector 1025 and will not further depress the corresponding resilient contact element 1024A. If the semiconductor wafer 1008 is driven further toward probe card 102 (shown in Figure 10), the overtravel stop protectors 1025 will press against terminals 222, driving space transformer 106 towards probe card 102. With sufficient drive force on semiconductor wafer 1008, probe card 102 will be deformed away from the semiconductor wafer. Designers can select stiffness properties for the probe card to accommodate expected probing force. One factor to consider is the number of resilient contact elements expected to contact the probe card assembly. Another factor is the spring constant of each spring. Another factor is to consider how much the probe card should yield when the probe card is overdriven. In general, if the spring constant per resilient contact element is k_s, then for n springs the effective spring rate of contacted springs is nk_s. In one preferred embodiment, the spring rate for the probe card k_{pcb} is greater than or equal to nk_s. It is particularly preferred that the k_{pcb} be on the order of 2 times nk_s.

One particularly preferred mode of operation is to have the overtravel stops evenly meet the probe card assembly then provide little or no additional force.

A general description of the device and method of using the present invention as well as a preferred embodiment of the present invention has been set forth above. One skilled in the art will recognize and be able to practice many changes in many aspects of the device and method described above, including variations which fall within the teachings of this invention. The spirit and scope of the invention should be limited only as set forth in the claims which follow.

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Claims

What is claimed is:

1. An apparatus for directly contacting an electronic component having raised contact elements (224), the apparatus comprising

a substrate (405) having a first substrate surface (118), and a first plurality of contact structures (222, 430, 336) mounted adjacent to the first substrate surface, and

a first plurality of contact connections (415, 331), and

a first plurality of connection elements (420), each connecting a one of the first plurality of contact structures to a corresponding one of the first plurality of contact connections.

2. The apparatus of claim 1 wherein the contact structures further comprise raised contact structures extending away from the substrate, and the raised contact structures are rigid.

3. The apparatus of claims 1 or 2 wherein the raised contact elements on the electronic component further comprise resilient contact structures.

4. The apparatus of claims 1, 2 or 3 wherein the apparatus is chip-scale, whereby it can directly contact a semiconductor device.

5. The apparatus of claims 1, 2 or 3 wherein the apparatus is package-scale, whereby it can directly contact a semiconductor-device package.

6. The apparatus of claims 1, 2 or 3 further comprising a plurality of contact regions, one on each contact structure, the plurality of contact regions substantially lying in plane.

7. The apparatus of claims 2, 3 or 6 wherein the raised contact structures extend away from the substrate far enough to provide clearance for the electronic component when the raised contact elements on the electronic component are brought into contact with the raised contact structures.

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8. The apparatus of claims 1, 2, 3 or 6 wherein the contact elements further comprise a contact layer including a material selected from the group consisting of nickel, palladium, cobalt, hard gold, soft gold, and rhodium.

9. The apparatus of claims 1, 2, 3 or 6 wherein the substrate further comprises a space transformer (106) having the first substrate surface (118), a second substrate surface, and a plurality of space transformer contact pads (120) disposed on the second substrate surface.

10. The apparatus of claim 9 wherein

each of the first plurality of contact structures are spaced one from another with a closest spacing of a first pitch between any two of the first plurality of contact elements, and

each of the plurality of space transformer contact pads are spaced one from another with a closest spacing of a second pitch between any two of the plurality of contact pads, and

the first pitch differs from the second pitch.

11. The apparatus of claim 10 wherein the second pitch is greater than the first pitch.

12. The apparatus of claims 1, 2, 3, 6, 9, 10 or 11 further comprising

a probe card (102, 321) having a first probe card surface, a second probe card surface and a plurality of probe card contact terminals (110, 332) on the first probe card surface, and the first plurality of contact connections (331) on the second probe card surface, and

the first plurality of connection elements each further comprising one or more component connection elements, each component connection element connected to another, so each connection element connects a one of the first plurality of contact structures to a corresponding one of the first plurality of contact connections.

13. The apparatus of claims 12 and any of claims 9, 10 or 11 further comprising

an interposer (104) having a first interposer surface (112), a second interposer surface, a first plurality of interposer resilient contact structures (116) extending from the

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first interposer surface and a second plurality of interposer resilient contact structures (114) extending from the second interposer surface; wherein

the first plurality of interposer resilient contact structures effect a pressure connection with the space transformer contact pads on the second substrate surface, and

the second plurality of interposer resilient contact structures effect a pressure connection with the probe card contact terminals of the probe card,

substantially each one of the first plurality of interposer resilient contact structures connecting a one of the space transformer contact pads to a corresponding one of the second plurality of interposer resilient contact structures and to a corresponding one of the probe card contact terminals,

each of the corresponding one of the first plurality of interposer resilient contact structures, one of the space transformer contact pads, one of the second plurality of interposer resilient contact structures, and one of the probe card contact terminals also acting as component connection elements.

14. The apparatus according to claims 12 or 13, further comprising

means (136, 138) for adjusting the orientation of the space transformer relative to the probe card without changing the orientation of the probe card.

15. The apparatus according to claim 14, wherein the means for adjusting the planarity of the space transformer comprises

an actuator, responsive to a computer, acting upon the space transformer.

16. The apparatus according to claims 12 or 13, further comprising

a plurality of differential screws, each including an outer differential screw element (136) and an inner differential screw element (138), acting upon the second surface of the space transformer, whereby one or more of the plurality of differential screws can be adjusted to adjust the orientation of the space transformer relative to the probe card without changing the orientation of the probe card.

17. The apparatus according to claims 1 or 2, further comprising terminals adjacent the first surface of the substrate wherein

the first plurality of contact structures (431, 430, 407) are mounted directly to terminals (410) on the first surface of the substrate.

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18. An assembly including the apparatus according to any claims 1-17 further comprising an electronic component (208, 310) having raised contact elements (224, 301), each raised contact element in contact with and electrical connection with a corresponding one of the first plurality of contact structures.

19. The assembly according to claim 18, wherein the raised contact elements are resilient contact elements and are under compression.

20. The assembly according to claim 19, wherein the raised contact elements have wiped across the corresponding contact structures.

21. The assembly according to claims 18, 19 or 20, wherein the electronic component comprises a semiconductor die (311).

22. The assembly according to claim 21, wherein the semiconductor die comprises a portion of a semiconductor wafer which has not been fully singulated.

23. The assembly according to claims 18, 19 or 20, wherein the electronic component comprises a package for a semiconductor device.

24. A method of using the apparatus according to any of claims 1-17, the method comprising bringing an electronic component (310) having raised contact elements (301) into contact with the contact structures, with a plurality of raised contact elements each in contact with and electrical connection with a corresponding one of the first plurality of contact structures.

25. The method according to claim 24, wherein the raised contact elements are resilient contact elements, the method further comprising compressing the resilient contact elements.

26. The method according to claim 24, further comprising wiping the raised contact elements across the corresponding contact structures.

27. The method according to claim 24, further comprising compressing the electronic component towards the substrate so that the probe card deforms and provides a spring force opposing the compression.

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28. A method of making the apparatus according to claims 2-17 having raised contact structures, the method comprising plating a raised contact structure over a terminal on the substrate.

29. The method according to claim 28 further comprising

providing the substrate, with a plurality of terminals adjacent the first surface of the substrate,

applying to the substrate a conductive layer (417, 407) of conductive material to establish an electrical connection to the plurality of terminals,

applying and patterning a layer of masking material (425) on the first surface of the substrate to provide openings over the plurality of terminals, and

depositing a first structural material (430) in the openings, in electrical contact with the plurality of terminals.

30. The method according to claim 29 further comprising

when depositing the first structural material in the openings, overfilling each opening, and

grinding back any excess first structural material so that a plurality of contact structures each have corresponding surfaces which lie substantially in the same plane.

31. The method according to claims 29 or 30 further comprising

depositing a contact material (431) over and in electrical contact with the first structural material.

32. The method according to claims 29, 30 or 31 further comprising

removing the masking material and at least some of the conductive layer of conductive material so that at least some of the plurality of contact structures each are isolated from electrical contact with others of the plurality of contact structures.

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Figure 1

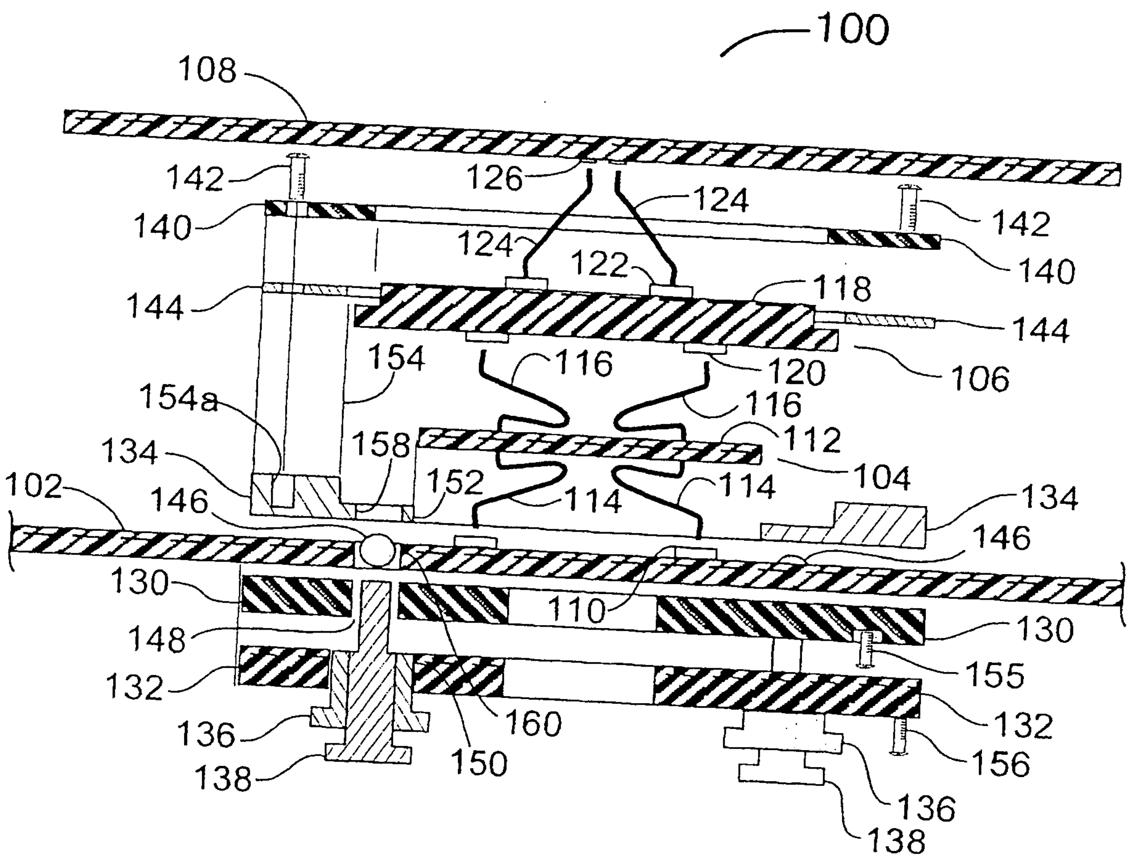

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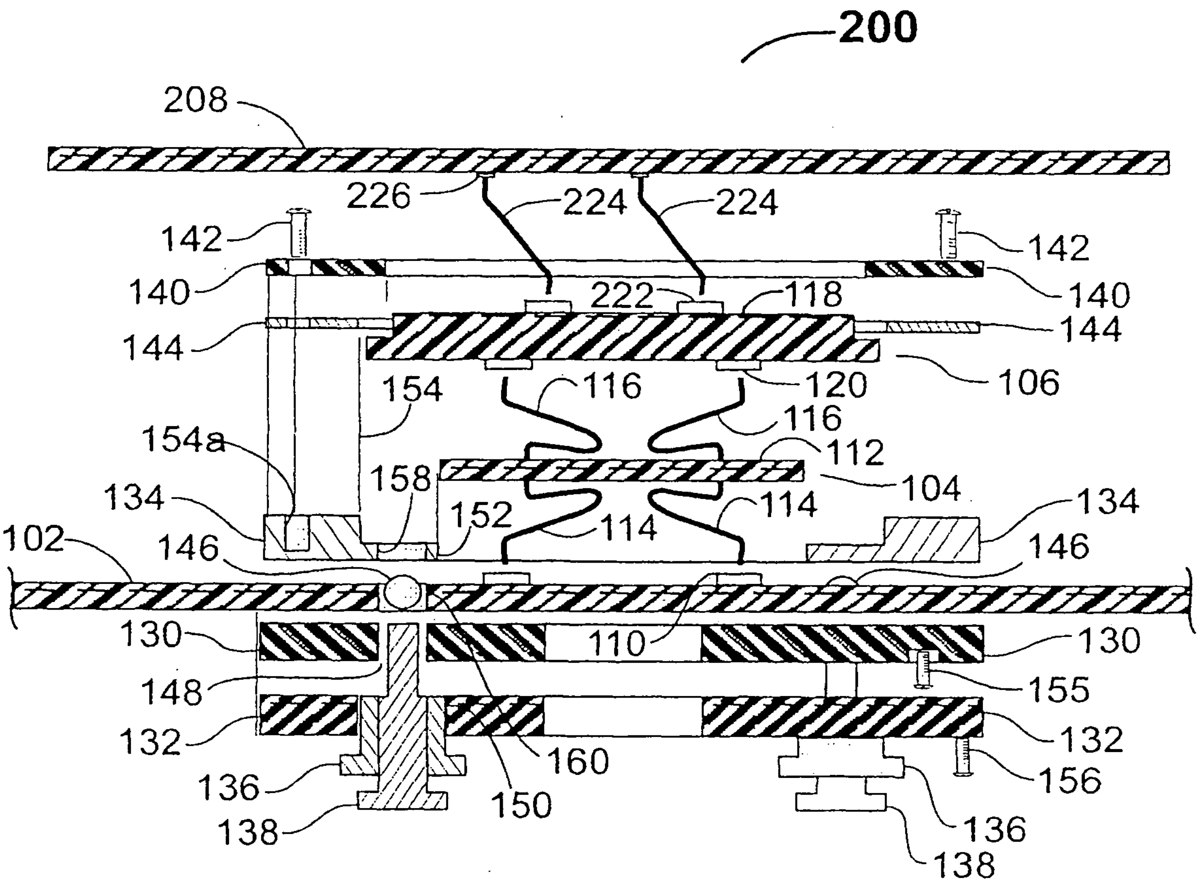
Figure 2



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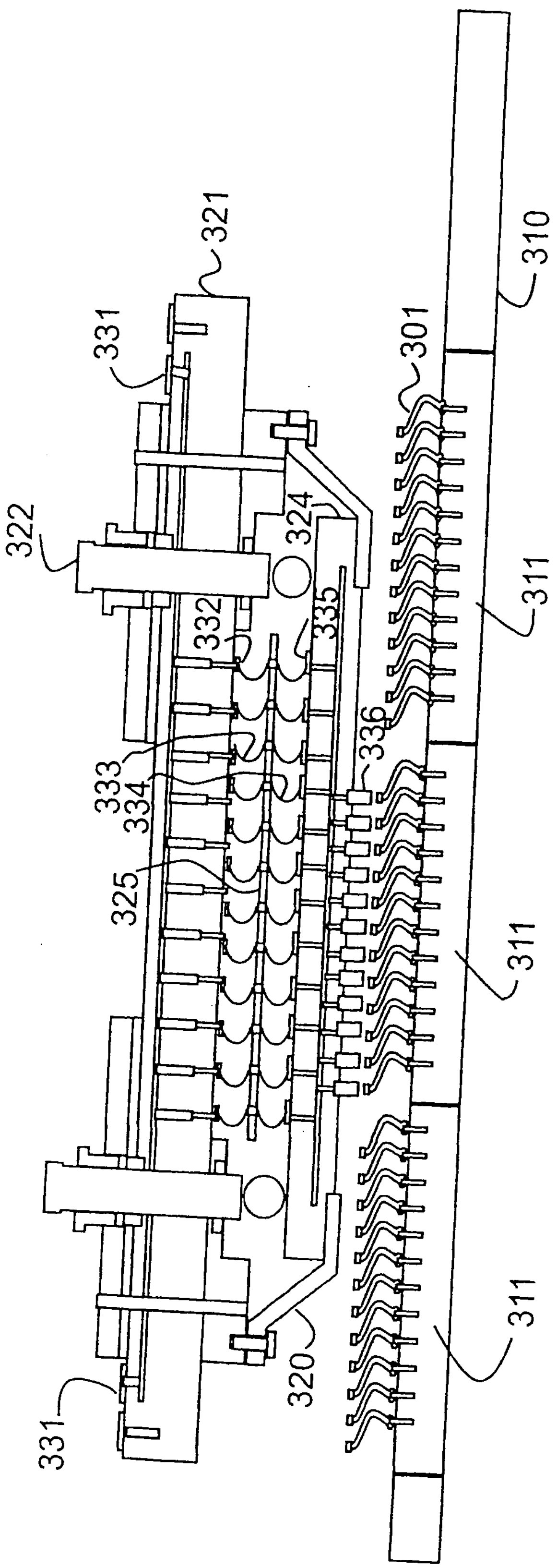

Fig. 3

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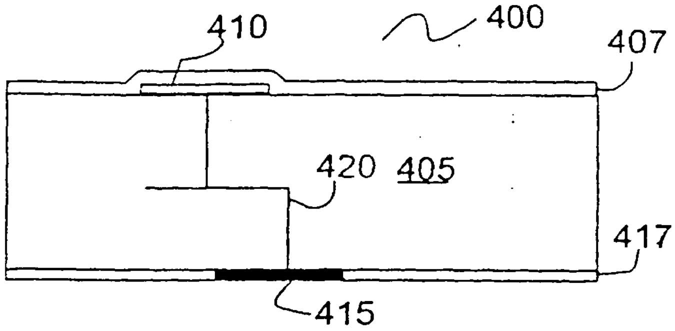

Fig. 4

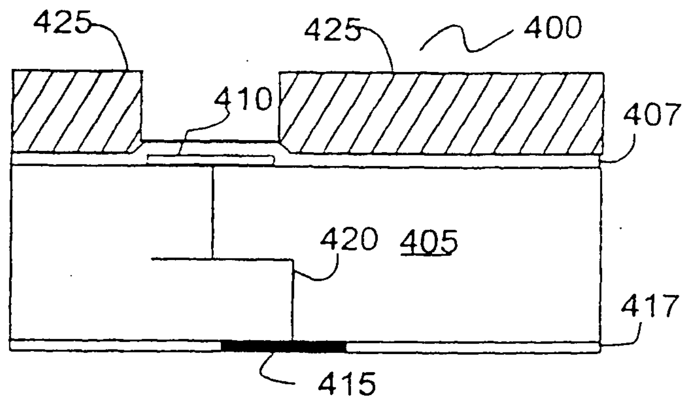

Fig. 5

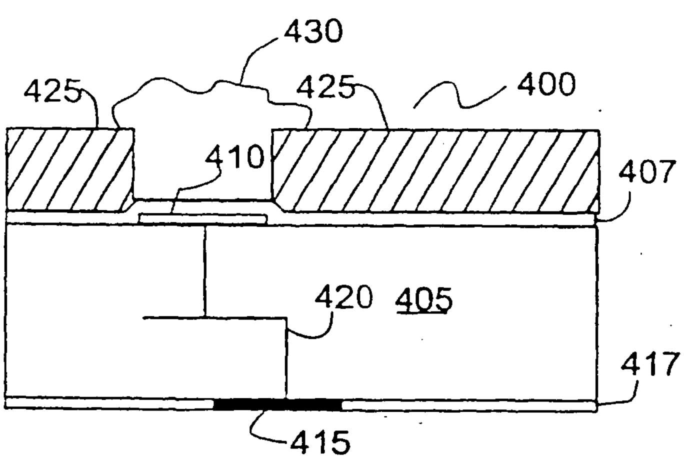

Fig. 6

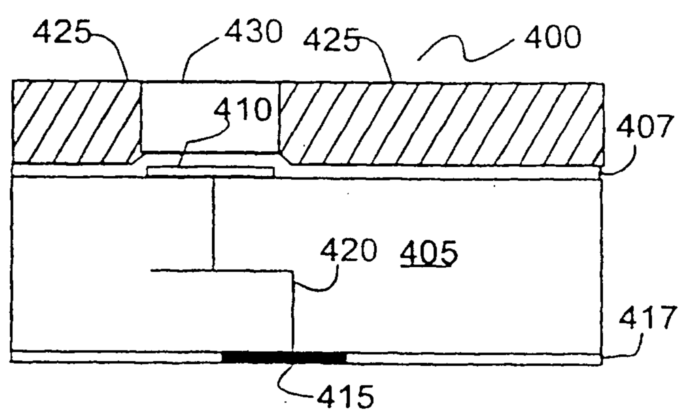

Fig. 7

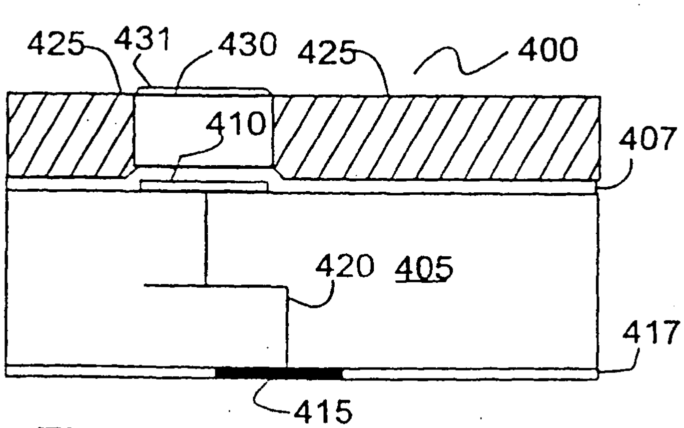

Fig. 8

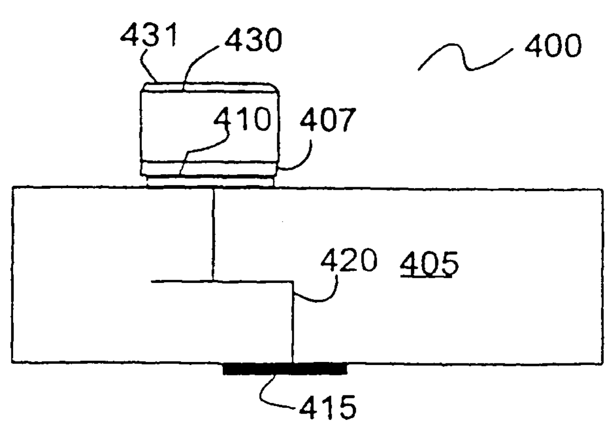

Fig. 9

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Figure 10

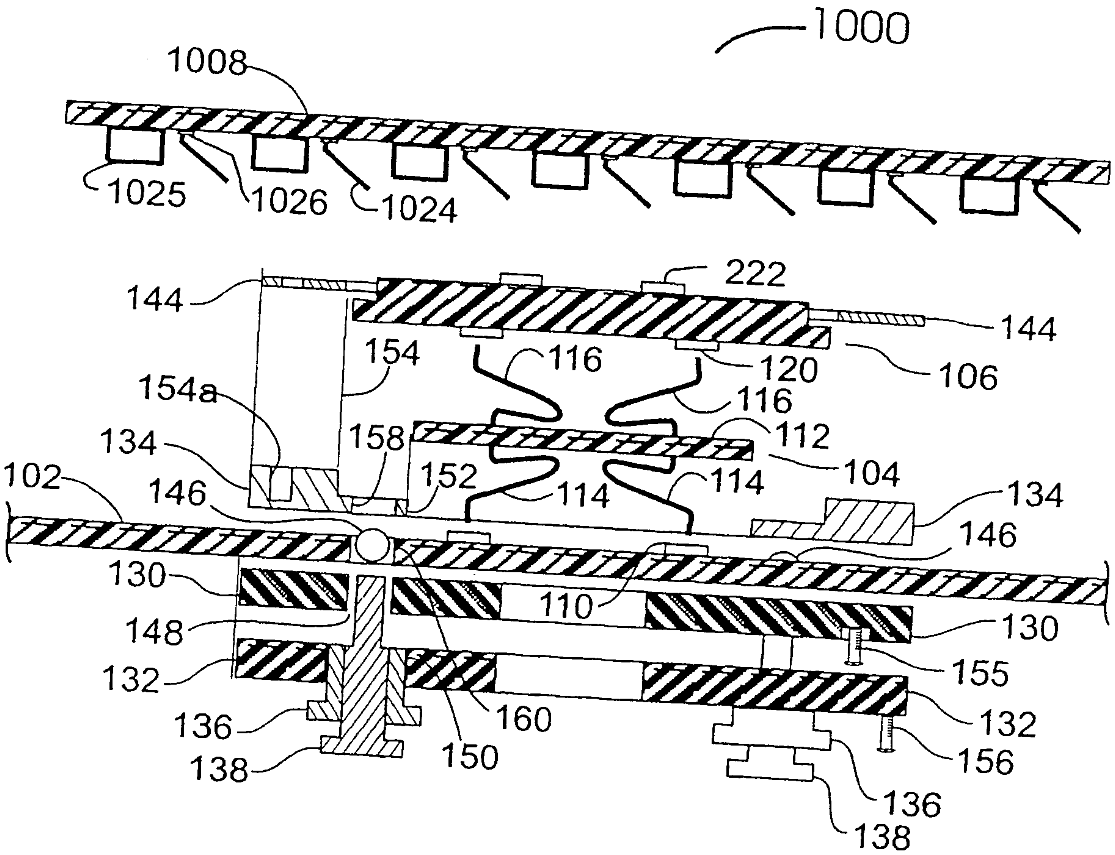
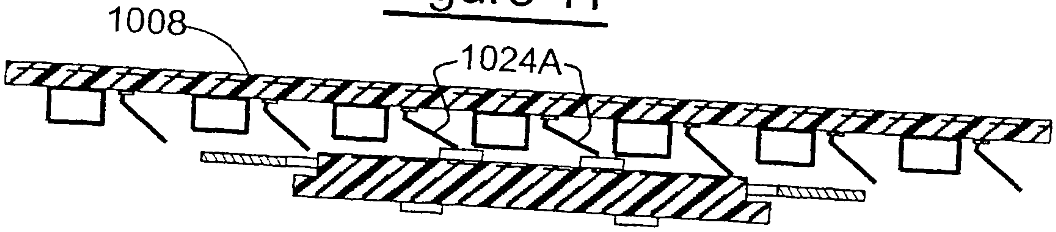


Figure 11



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INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 99/28746

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G01R31/316

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G01R

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 96 15458 A (FORMFACTOR) 23 May 1996 (1996-05-23) cited in the application claims 1-42; figures 5,7	1-32
X	WO 98 21597 A (CHARMANT BEHEER B.V.) 22 May 1998 (1998-05-22) figure 1	1
X	US 5 821 763 A (BEAMAN ET AL.) 13 October 1998 (1998-10-13) claim 1; figure 6	1
A	US 5 701 085 A (MALLADI ET AL.) 23 December 1997 (1997-12-23) figure 2	1

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
11 April 2000	17/04/2000

Name and mailing address of the ISA	Authorized officer
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INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 99/28746

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No
A	EP 0 632 281 A (PLESSEY) 4 January 1995 (1995-01-04) figure 2 -----	1

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